CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. A method for analyzing a virtual layout of a semiconductor chip, comprising:

scanning a virtual layout to encounter a first object having an x-coordinate and a y-coordinate;

determining whether the y-coordinate of the first object is beyond a y-coordinate of a second object that has an x-coordinate and the y-coordinate stored in a cache; and

discarding the x-coordinate and the y-coordinate of the second object from the cache if the y-coordinate of the first object is beyond the y-coordinate of the second object.

2. The method of claim 1, further including, responsive to determining that the y-coordinate of the first object is not beyond the y-coordinate of the second object, storing the x-coordinate and the y-coordinate of the first object in the cache.

3. The method of claim 2, further including detecting for the presence of a design flaw between the first object and the second object.

4. The method of claim 3, wherein the design flaw includes at least one of touches between objects, overlaps between objects.

5. The method of claim 3, wherein the detecting occurs across at least one of a single layer and multiple layers.

6. The method of claim 1, further including reporting the design flaw.

7. The method of claim 1, wherein the first object and the second object include geometric objects of a virtual layout, the geometric objects representing structures in a microchip.

8. A method for analyzing a virtual layout of a semiconductor chip, comprising:

scanning a virtual layout using a semi-greedy algorithm; and

detecting an event.

9. The method of claim 8, further including reporting the event.

10. The method of claim 8, wherein the event includes at least one of touches between objects, overlaps between objects, last encounter with an object, first encounters with an object, a parameter of an object.

11. A system for scanning a virtual layout of a microchip design, comprising:

scan and detection logic configured to scan a virtual layout to encounter a first object having first coordinates, store a second object having second coordinates in a cache, determine whether the first coordinates are outside the range of the second coordinates, and discard the second coordinates from the cache if the first coordinates are outside the range of the second coordinates.

12. The system of claim 11, wherein the scan and detection logic are comprised of instantiations of at least one of an axon class, a dendrite class included in the axon class, an active domains class included in the dendrite class, a domain class included in the dendrite class, a traversal engine class configured to perform scan traversals of the virtual layout, and a rectangle iterator class that manages the scan traversals over multiple objects of the virtual layout.

13. The system of claim 12, wherein the instantiations of the axon class, the dendrite class, the active domains class, the domain class, the traversal engine class, and the rectangle iterator class are each configured as independent modules.

14. The system of claim 12, wherein the instantiations of the axon class, the dendrite class, the active domains class, the domain class, the traversal engine class, and the rectangle iterator class are collectively configured as a single module.

15. The system of claim 12, wherein the instantiations of the domain class includes a state that is updated for each scan line change.

16. The system of claim 12, wherein the instantiations of the dendrite class includes instantiations of multiple domain classes, wherein each instantiation of the domain class corresponds to an object in the virtual layout.

17. The system of claim 12, wherein the scan and detection logic is further configured to, responsive to determining that the first coordinates are not outside the range of the second coordinates, store the first coordinates in the cache.

18. The system of claim 17, wherein the scan and detection logic is further configured to detect whether an instantiation of a domain class corresponding to the first object includes coordinates that give rise to a design flaw with coordinates included in an instantiation of a domain class corresponding to the second object.

19. The system of claim 12, wherein the scan and detection logic are configured to discard a state of the domain object corresponding to the second coordinates.

20. The system of claim 11, wherein the scan and detection logic are configured in a digital signal processor.

21. The system of claim 11, wherein the scan and detection logic are configured as software in communication with a processor.

22. A scan and detection system comprising:

means for traversing a virtual layout of a microchip design;

means for detecting whether a first object has coordinates within a range of coordinates of a second object stored in a cache; and

means for discarding the coordinates of the second object when the first object has coordinates outside the range of coordinates of the second object.

23. The system of claim 22, further including means for storing the coordinates of the first object in the cache.

24. The system of claim 23, further including means for detecting a design flaw between the first object and the second object.

25. A computer readable medium having a computer program for scanning and detecting connectivity between structures in a virtual layout, the program comprising:

logic configured to scan objects of a virtual layout using a semi-greedy algorithm; and

logic configured to detect an event.

26. The computer readable medium of claim 25, wherein the logic includes data structures that reference the objects of the virtual layout.

27. The computer readable medium of claim 26, wherein the data structures are configured as at least one of a linked list, a tree list, and classes.